

# ML4022-LB-V1

## Technical Reference

**SFP-DD Electrical Passive Loopback Module**  
MSA Compliant (MIS Rev0.2)



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## 1 Overview

The **ML4022-LB** SFP-DD Passive Electrical Loopback is used for testing SFP-DD transceiver ports under board level tests. The **ML4022-LB** provides a cost-effective low loss method for SFP-DD port testing by acting as a substitute for a fully-featured SFP-DD transceiver.

The **ML4022-LB** is packaged in a standard MSA housing compatible with all SFP ports. High speed signals are electrically looped back from TX side to RX side of the module, the differential TX pair is connected to the corresponding RX pair, and the signals are AC coupled as specified by SFP-DD MSA HW specs.

### 1.1 ML4022-LB SFP-DD Thermal Load | Key Features

- Power Consumption up to 4.96 W, spread over 4 spots
- Dual channels, supporting up to 28 Gbaud each (56 Gbps)
- LED indicator
- Custom Memory Maps
- Temperature range from 0 °C to 80 °C for regular, and -40 °C to 85 °C for IND
- I2C Interface
- MSA Compliant EEPROM
- Voltage sense
- Temperature sense
- Insertion Counter
- Micro controller based

### 1.2 Recommended Operating Conditions

Parameter	Symbol	Notes/Conditions	Min	Typ	Max	Units
Operating Temperature	T <sub>A</sub>		0		80	°C
Supply Voltage	VCC	Main Supply Voltage	3.00	3.3	3.6	V
Data Rate	R <sub>b</sub>	Guaranteed to work at 56 Gbps	0		56	Gbps
Input/Output Load Resistance	RL	AC-Coupled, Differential	90	100	110	Ω
Power Class		Programmable to Emulate all power classes	0	-	4.96	W

## 2 Ordering Information

### 2.1 Ordering Options

MultiLane provides two different part numbers for the **ML4022-LB**, differing in the power spots distribution and the maximum power dissipation. Ordering Part Numbers are described in the table below.

Option	Description
<b>ML4022-LB-V1</b>	Maximum power spots dissipation: 4.32 W
<b>ML4022-LB-5W-V1</b>	Maximum power spots dissipation: 4.96 W

### 2.2 LED Indicator

**Green** - Signifies that the module is plugged-in and operating in high power mode as defined by the SFP-DD MSA specification.

**Red** - Signifies the module is plugged-in and operating in low power mode as defined by the SFP-DD MSA specifications.

## 3 Functional Description

### 3.1 Management Data Interface – I2C

The **ML4022-LB** supports the I2C interface. This SFP-DD specification is based on the SFF-8419.

### 3.2 I2C Signals, Addressing and Frame Structure

#### 3.2.1 I2C Frame

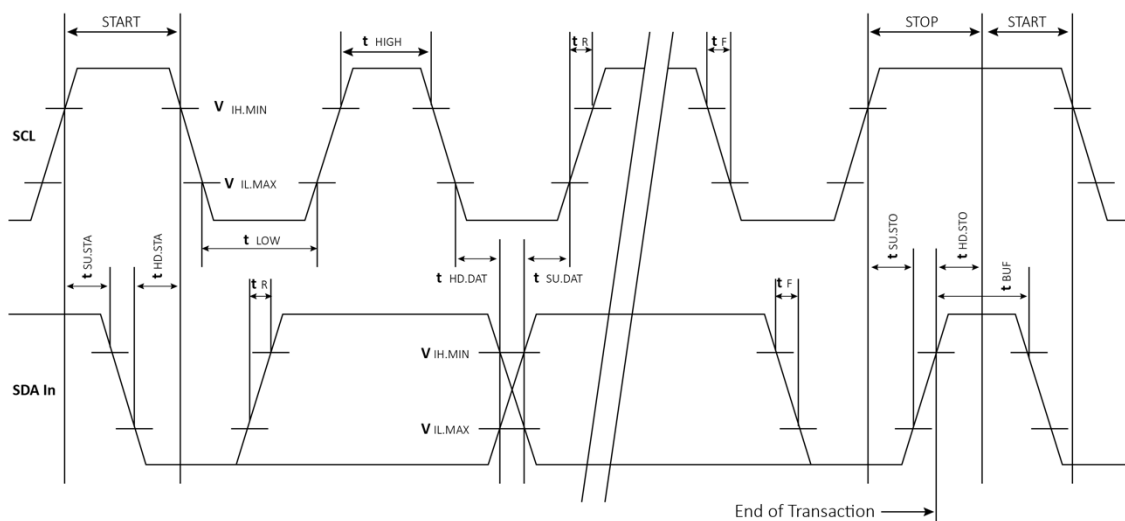


Figure 1: I2C Frame

The 2-wire serial interface address of the SFP-DD module is A0h.

### 3.2.2 Management Timing Parameters

Parameter	Symbol	Min	Max	Unit
Clock Frequency	$f_{SCL}$	0	400	kHz
Clock Pulse Width Low	$t_{LOW}$	1.3		ns
Clock Pulse Width High	$t_{High}$	0.6		ns
Time bus free before new transmission can start	$t_{BUF}$	20		us
Input Rise Time (400 kHz)	$t_{R,400}$		300	ns
Input Fall Time (400 kHz)	$t_{F,400}$		300	ns
Serial Interface Clock Holdoff "Clock Stretching"	$T_{\_clock\_hold}$		500	us

### 3.2.3 Device Addressing and Operation

**Clock and Data Transitions:** The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition. All addresses and data words are serially transmitted to and from the SFP-DD in 8-bit words. Every byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

**START Condition:** A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

**STOP Condition:** A low-to-high transition of SDA with SCL high is a STOP condition.

**Acknowledge:** After sending each 8-bit word, the transmitter releases the SDA line for one bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host should be acknowledged by SFP-DD transceiver. Read data bytes transmitted by SFP-DD transceiver should be acknowledged by the host for all but the final byte read, for which the host should respond with a STOP instead of an ACK.

**Memory (Management Interface) Reset:** Synchronization issues may cause the master and slave to disagree on the specific bit location currently being transferred, the type of operation or even if an operation is in progress. The TWI protocol has no explicitly defined reset mechanism. The following procedure may force completion of the current operation and cause the slave to release SDA.

Clock up to 9 cycles.



Once acknowledged by the SFP-DD, the current address data word is serially clocked out. The host does not respond with an acknowledgement, but does generate a STOP condition once the data word is read.

### 3.3.2.2 Random Read

A random read operation requires a “dummy” write operation to load in the target byte address as shown in Figure 3 below. This is accomplished by the following sequence.

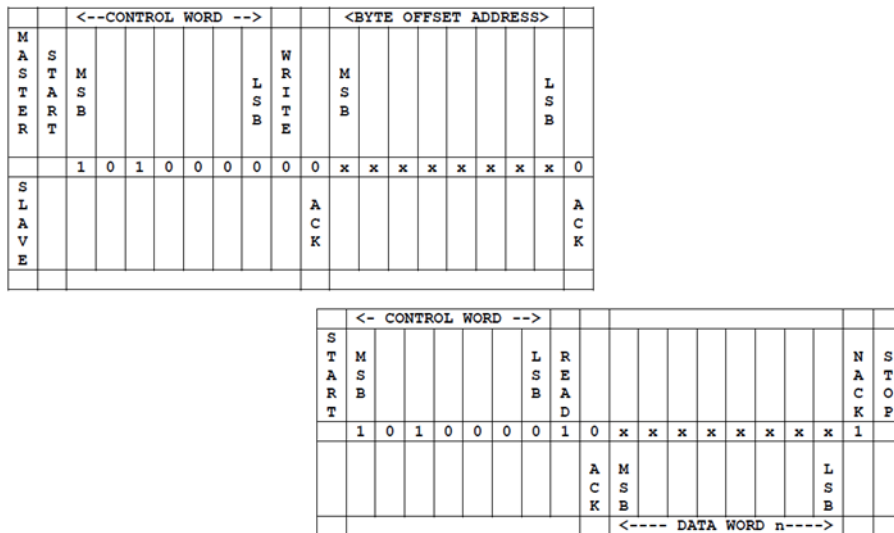


Figure 3: SFP-DD Random Read

The target 8-bit data word address is sent - following the device address write word (10100000) - and acknowledged by the SFP-DD. The host then generates another START condition - aborting the dummy write without incrementing the counter - and a current address read by sending a device read address (10100001). The SFP-DD acknowledges the device address and serially clocks out the requested data word. The host does not respond with an acknowledgement, but does generate a STOP condition once the data word is read.

### 3.3.2.3 Sequential Read

Sequential reads are initiated by a current address read (Figure 4) or a random address read (Figure 5). To specify a sequential read, the host responds with an acknowledgement (instead of a STOP) after each data word. As long as the SFP-DD receives an acknowledgement, it shall serially clock out sequential data words. The sequence is terminated when the host responds with a NACK and a STOP instead of an acknowledgement.









### 3.4 SFP-DD Memory Map

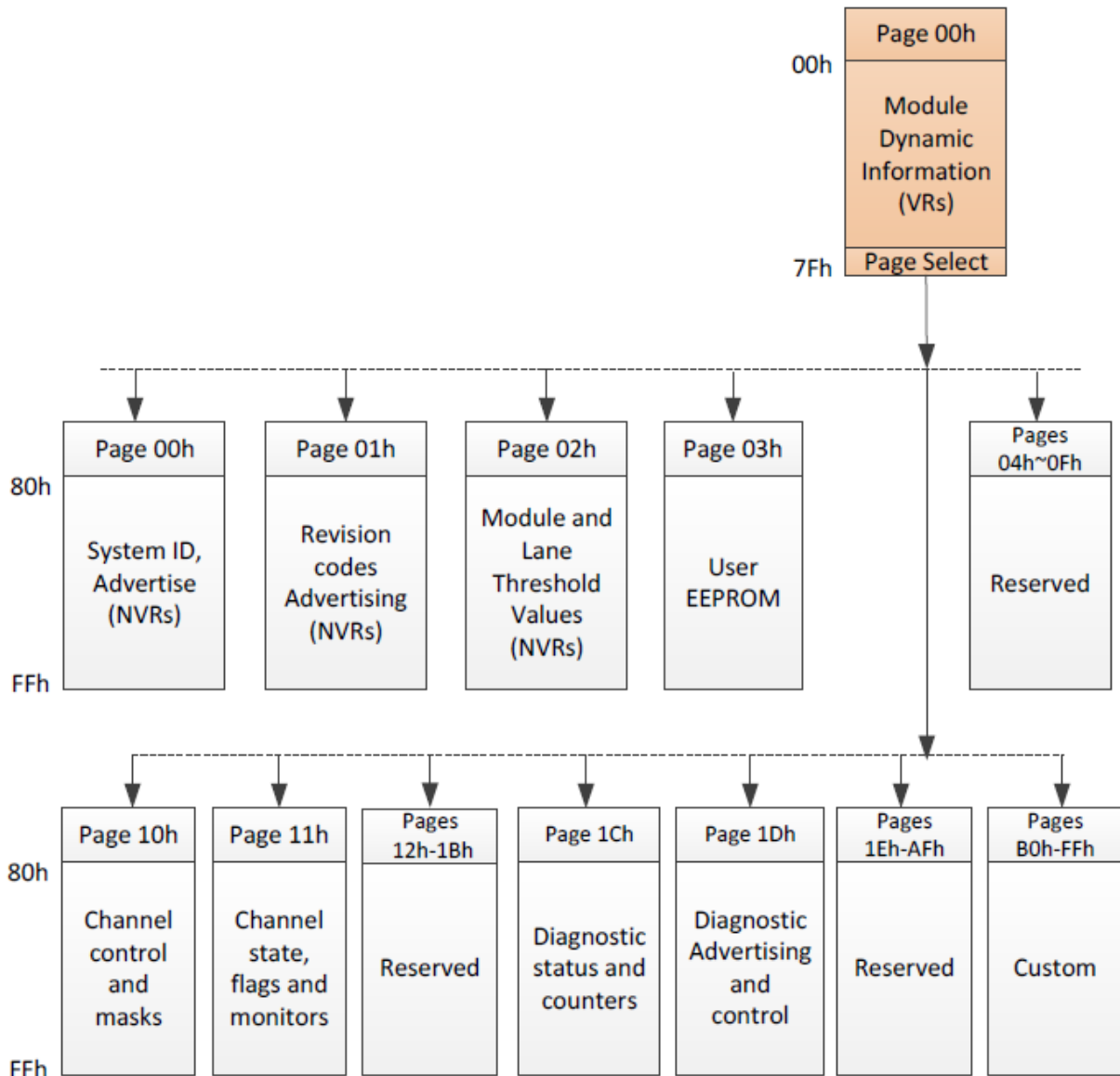


Figure 8: SFP-DD Memory Map

### 3.5 Low Speed Electrical Hardware Pins

In addition to the 2-wire serial interface the module has the following low speed pins for control and status:

- TxFault0, TxFault1
- TxDisable0, TxDisable1
- LPMODE
- Speed0-1, Speed0-2, Speed1-1, Speed1-2
- RxLOS0, RxLOS1

### 3.5.1 TxFault0, TxFault1

TxFault0 and TxFault1 are module outputs, the **ML4022-LB** provides control functionality for those outputs by writing to bits 5~4 of register 143 (page 03).

Address	Bit	Name	Description	Type
143 (Page 03)	4	TxFault0 control bit	1b= TxFault0 set High 0b= TxFault0 set Low	RW
	5	TxFault1 control bit	1b= TxFault1 set High 0b= TxFault1 set Low	

### 3.5.2 TxDisable0, TxDisable1

TxDisable0 and TxDisable1 are module inputs from the Host, the digital state of those input signals can be checked via register 141 (Page 03) as shown below.

Address	Bit	Name	Description	Type
141 (Page 03)	0	TxDisable0	Digital State: Read 0b: signal is Low Read 1b: signal is High	RO
	1	TxDisable1		
	4	TxDisable0	Transition Detection: Read 0b: No edge detected Read 1b: Either rising or falling edges detected Write 0b: No effect Write 1b: Clear the register	
	5	TxDisable1		

### 3.5.3 LPMode

LPMode is an input signal to the module from the host operating with active high logic. The LPMode signal is pulled up to Vcc in the SFP-DD module. The LPMode signal intervenes in the Module State Transition (refer to section [3.6.2](#) for more details).

Address	Bit	Name	Description	Type
139 (Page 03)	0	LP Mode	Digital State: Read 0b: signal is Low Read 1b: signal is High	RO
	4		Transition Detection: Read 0b: No edge detected Read 1b: Either rising or falling edges detected Write 0b: No effect Write 1b: Clear the register	

### 3.5.4 Speed0-1, Speed0-2, Speed1-1, Speed1-2

Speed0-1, Speed0-2, Speed1-1 and Speed1-2 are module inputs. Digital state of those signals can be checked via register 142 (Page 03).

Address	Bit	Name	Description	Type
141 (Page 03)	0	Speed0-1	Digital State: Read 0b: signal is Low Read 1b: signal is High	RO
	1	Speed0-2		
	2	Speed1-1		
	3	Speed1-2		
	4	Speed0-1	Digital State: Read 0b: signal is Low Read 1b: signal is High Transition Detection:	
	5	Speed0-2	Read 0b: No edge detected Read 1b: Either rising or falling edges detected	
	6	Speed1-1	Write 0b: No effect Write 1b: Clear the register	
	7	Speed1-2		

### 3.5.5 RxLOS0, RxLOS1

RxLOS0 and RxLOS1 are module output signals.

These two signals could be controlled using two modes:

1. Following TxDisable state
2. Direct signal control

#### 3.5.5.1 Following TxDisable

Address	Bit	Name	Description	Type
143 (Page 03)	0	RxLOS0 control source	1b= RXLOS0 follows digital state of TxDisable0 0b= RXLOS0 controlled directly through bit 1	RW
	2	RxLOS1 control source	1b= RXLOS1 follows digital state of TxDisable1 0b= RXLOS1 controlled directly through bit 3	

### 3.5.5.2 Direct Control

Address	Bit	Name	Description	Type
143 (Page 03)	0	RxLOS0 control bit	1b= RXLOS0 set high 0b= RXLOS0 set Low	RW
	2	RxLOS1 control bit	1b= RXLOS1 set high 0b= RXLOS1 set Low	

## 3.6 ML4022-LB Specific Functions

### 3.6.1 Module State

The Module State describes module-wide behaviors and properties. The **ML4022-LB** implements two module states: ModuleReady and ModuleLowPwr.

The ModuleLowPwr state is a host control state, where the management interface is fully initialized and operational and the device is in Low Power mode, the LED turns Red and the PWM is deactivated. During this state, the host may configure the module using the management interface and memory map. The module state encoding for ModuleLowPwr is 001.

The ModuleReady state is a host control state that indicates that the module is in High Power mode, the LED turns Green and the PWM is activated. The module state encoding for ModuleReady is 011.

Address	Bit	Name	Description	Type
3 (lower Page)	3~1	Module State	Current state of Module: 001b= ModuleLowPwr 011b= ModuleReady	RO

### 3.6.2 Module State Transition

The state transition between Low Power and High Power is related to three parameters:

1. ForceLowPwr bit– software control (forces module into low power mode), register 26 bit 4
2. LowPwr bit – software control, register 26 bit 6
3. LPMode – Hardware signal

According to these parameters, the state of the module is defined. Conditions for Low Power and High Power state, are summarized in the table below.

ForceLowPwr ( Reg 26 bit 4)	LowPwr (register 26 bit 6)	LPMode	State
1	X	X	Low Power
0	1	1	Low Power
0	1	0	High Power

0	0	1	High Power
0	0	0	High Power

### 3.6.3 Module Global Controls

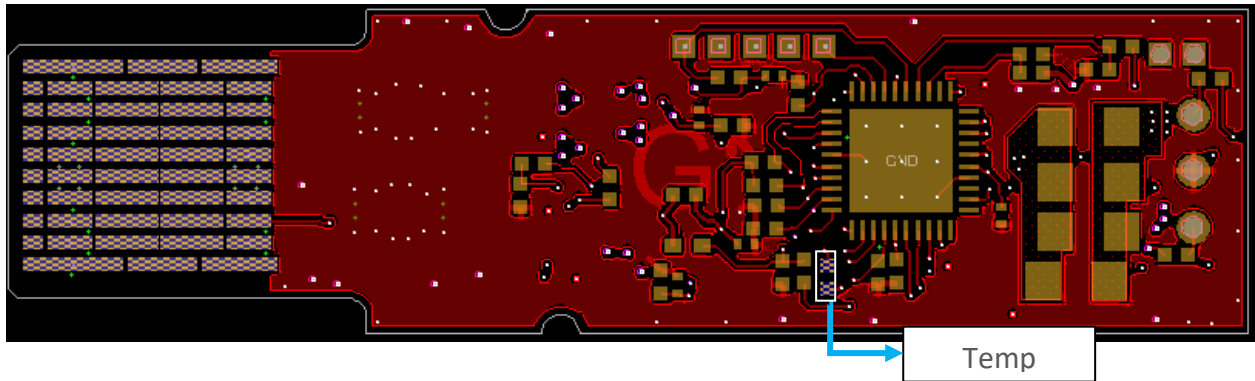
Module global controls are control aspects that are applicable to the entire module or all channels in the module.

Address	Bit	Name	Description	Type
26(lower Page)	6	LowPwr	Parameter used to control the module power mode (refer to section 3.6.2) Default value =1	RW
	4	ForceLowPwr	0b= high power mode(default) 1b=Forces module into low	
	3	Software Reset	Self-clearing bit that causes the module to be reset. The effect is the same as asserting the reset pin for the appropriate hold time, followed by its de-assertion. This bit will be cleared to zero on a reset so a value of 0 will always be returned. 0b=not in reset 1b=Software reset	
3(lower page)	0	Software Interrupt	Digital state of Interrupt: 0b= Interrupt source is present 1b= No interrupt source present	RO

### 3.6.4 Temperature Monitor

The **ML4022-LB** has an internal temperature sensor in order to continuously monitor the module temperature. The temperature sensor readings are present in low-memory registers 14-15. Internally measured Module temperature are represented as a 16-bit signed two's complement value in increments of 1/256 °C, yielding a total range of -127 °C to +128 °C that is considered valid between -40 °C and +85 °C. Temperature accuracy is less than 1 °C over specified operating temperature and voltage. The location of the temperature sensor is shown below.

Address	Bit	Name	Description	Type
14 (lower Page)	All	Temperature MSB	Internally measured TempSense4 (shell T.S.)	RO
15 (lower Page)	All	Temperature LSB	Internally measured TempSense4 (shell T.S.)	



The temperature Alarms' and warnings' interrupt flags exist in lower page.

Address	Bit	Name	Description
9 (lower Page)	3	L-Temp Low Warning	Latched low temperature warning flag
	2	L-Temp High Warning	Latched high temperature warning flag
	1	L-Temp Low Alarm	Latched low temperature alarm flag
	0	L-Temp High Alarm	Latched high temperature alarm flag

Note that any interrupt flag when asserted will generate the interrupt. Its state is read from register 3 bit 0 (refer to the table in section [3.6.3](#)).

### 3.6.5 Programmable Power Dissipation & Thermal Emulation

Registers 135, 136, 137 and 138, Page 03h are all 8-bit wide and are used for PWM control over I2C. The consumed power changes accordingly when the values of these registers are changed (only in high power mode). In Low power mode the module automatically turns off PWM. The values written in these registers are permanently stored.

The PWM can also be used for module thermal emulation.

The module contains 4 thermal spots positioned where the optical transceivers usually are in an optical module that is heated relative to the related PWM register.

The maximum power dissipation and distribution differ depending on the module part number, as described in the following sections



### 3.6.5.1 ML4022-LB-V1

In the **ML4022-LB-V1** part number, each spot is 1.08 W. Programmable power can be controlled using PWM, thus allowing a power consumption that covers all the range from 0 to 4.32 W with 4.2 mW resolution.

Note that these values are the NET spots consumption, where the module components dissipate around 0.14 W, which is added to spots power to get total module consumption.

Address	Bit	Name	Description
<b>135 (Page 03)</b>	7:0	PWM controller 1	1.08 W Top power spot control register, powered by VccR net
<b>136 (Page 03)</b>	7:0	PWM controller 2	1.08 W Top power spot control register, powered by VccT net
<b>137 (Page 03)</b>	7:0	PWM controller 3	1.08 W Bottom power spot control register, powered by VccR net
<b>138 (Page 03)</b>	7:0	PWM controller 4	1.08 W Top power spot control register, powered by VccT net

In the figure below, the red spots represent the thermal spots of the **ML4022-LB-V1** module.

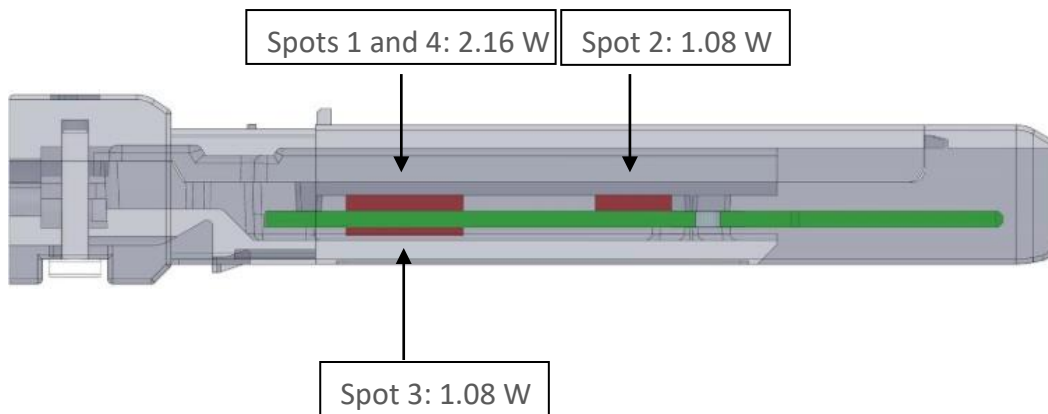


Figure 9: ML4022-LB-V1 Power Spots Location

### 3.6.5.2 ML4022-LB-5W-V1

In the **ML4022-LB-5W-V1** part number, spots 1 and 3 are 1.4 W each, and spots 2 and 4 are 1.08 W each. Programmable power can be controlled using PWM, thus allowing a power consumption that covers all the range from 0 to 4.96 W.

Note that these values are the NET spots consumption, where the module components dissipate around 0.14 W, which is added to spots power to get total module consumption.

Address	Bit	Name	Description
<b>135 (Page 03)</b>	7:0	PWM controller 1	1.4 W Top power spot control register, powered by VccR net
<b>136 (Page 03)</b>	7:0	PWM controller 2	1.08 W Top power spot control register, powered by VccT net

137 (Page 03)	7:0	PWM controller 3	1.4 W Bottom power spot control register, powered by VccR
138 (Page 03)	7:0	PWM controller 4	1.08 W Top power spot control register, powered by VccT net

In the figure below, the red spots represent the thermal spots of the **ML4022-LB-5W-V1** module.

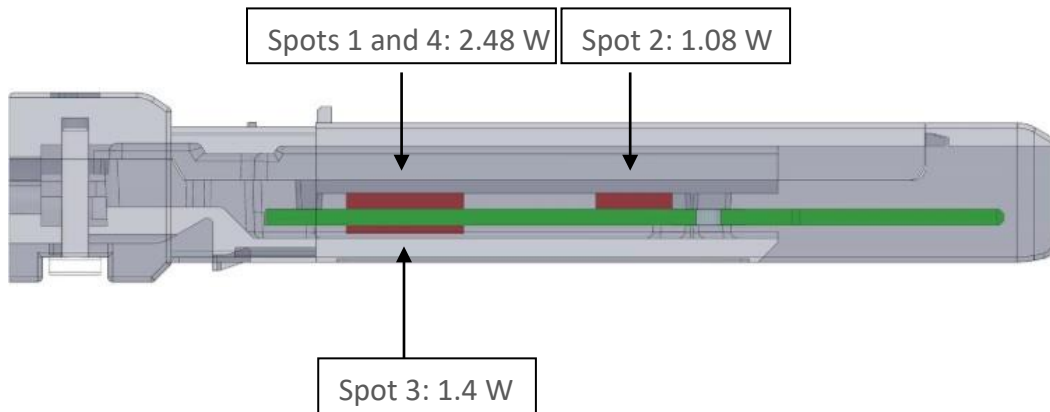


Figure 10: ML4022-LB-5W-V1 Power Spots Location

### 3.6.6 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is pre-defined.

The module is continuously monitoring the temperature and checking its value against the Cut-Off temperature. Once the module reaches the cut-off temperature, the PWM will automatically turn off in order to prevent overheating. Once the temperature is 5 °C below cut-off value, the PWM turns on again with the same previous values.

The Cut-Off temperature for the **ML4022-LB** is 85 °C and it can be programmed to any value from register 134 of memory Page 03. Maximum cut-off temperature is 90 °C.

Address	Bit	Name	Description	Type
134 (Page 03)	7:0	Cut-Off temperature	Module Cut-Off Temperature, LSB = 1 °C	RW

### 3.6.7 Voltage Sense

The **ML4022-LB** features two voltage sense circuits that allow measuring of internal module voltages VccT and VccR. Measured values range from 0 to 6.55 V. LSB unit is 100 μV.

Address	Bit	Name	Description
16 (lower Page)	ALL	VccR MSB	Internally measured module VccR
17 (lower Page)	ALL	VccR LSB	Internally measured module VccR
22 (lower Page)	ALL	VccT MSB	Internally measured module VccT

23 (lower Page)	ALL	VccT LSB	Internally measured module VccT
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The Voltage Alarms and warnings interrupt flags exists in lower Page.

Address	Bit	Name	Description
9 (lower Page)	7	L-VCCR Low Warning	Latched low supply voltage warning flag
	6	L-VCCR High Warning	Latched low supply voltage warning flag
	5	L-VCCR Low Alarm	Latched low supply voltage alarm flag
	4	L-VCCR High Alarm	Latched low supply voltage alarm flag

Address	Bit	Name	Description
11 (lower Page)	3	L-VCCT Low Warning	Latched low supply voltage warning flag
	2	L-VCCT High Warning	Latched low supply voltage warning flag
	1	L-VCCT Low Alarm	Latched low supply voltage alarm flag
	0	L-VCCT High Alarm	Latched low supply voltage alarm flag

### 3.6.8 Insertion Counter

The Insertion counter contains the number of times the module was plugged in a host. The insertion counter is incremented every time the module goes in initializing sequence, as it is nonvolatile it is always saved. The insertion counter can be read from registers 132-133 Page 03.

Address	Bit	Name	Description
132 (Page 03)	MSB	Insertion Counter MSB	
133 (Page 03)	LSB	Insertion Counter LSB	LSB unit = 1 insertion

### 3.6.9 Alarm and Warning Thresholds

Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory-preset values allow the user to determine when a particular value is exceeding the predefined limit. While Voltage LSB unit is 100  $\mu$ V and Temperature LSB unit is 1/256  $^{\circ}$ C. Note that these addresses are of memory Page 02.

Address	Bit	Name	Description	Type
128(Page 02)	ALL	high temp alarm threshold (MSB)	80 $^{\circ}$ C	RW
129(Page 02)	ALL	high temp alarm threshold (LSB)		
130(Page 02)	ALL	low temp alarm threshold (MSB)	0 $^{\circ}$ C	
131(Page 02)	ALL	low temp alarm threshold (LSB)		

<b>132(Page 02)</b>	ALL	high temp warning threshold (MSB)	75 °C	
<b>133(Page 02)</b>	ALL	high temp warning threshold (LSB)		
<b>134(Page 02)</b>	ALL	low temp warning threshold (MSB)	5 °C	
<b>135(Page 02)</b>	ALL	low temp warning threshold (LSB)		
<b>136(Page 02)</b>	ALL	high volt alarm threshold (MSB)	3.6 V	
<b>137(Page 02)</b>	ALL	high volt alarm threshold (LSB)		
<b>138(Page 02)</b>	ALL	low volt alarm threshold (MSB)	3.0 V	
<b>139(Page 02)</b>	ALL	low volt alarm threshold (LSB)		
<b>140(Page 02)</b>	ALL	high volt warning threshold (MSB)	3.55 V	
<b>141(Page 02)</b>	ALL	high volt warning threshold (LSB)		
<b>142(Page 02)</b>	ALL	low volt warning threshold (MSB)	3.05 V	
<b>143(Page 02)</b>	ALL	low volt warning threshold (LSB)		

### 3.6.10 FW and HW Revision

Information about the FW and HW revision are present in lower page registers 39 and 40, and in Page 01, registers 130 and 131 as described in the table below.

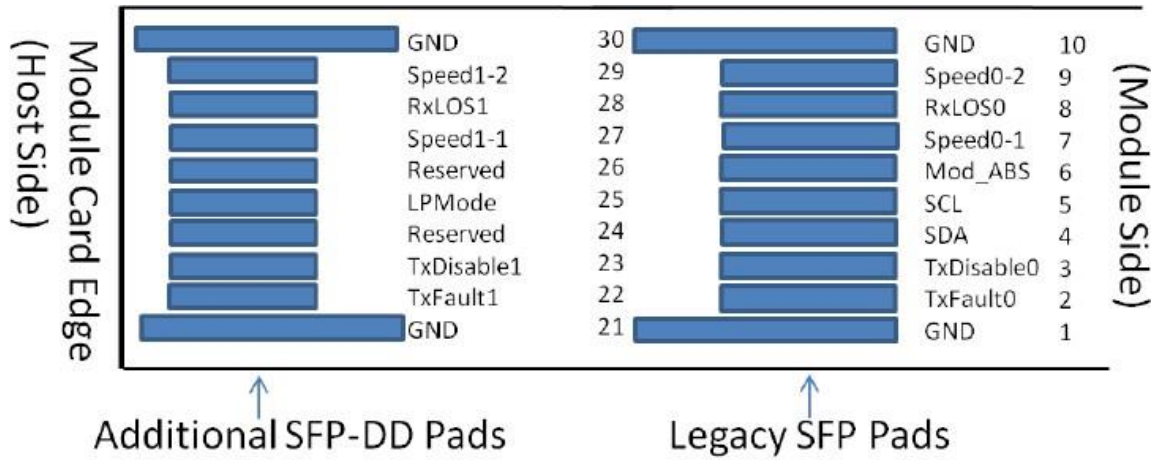
Address	Bit	Name	Type
<b>39 (Lower Page)</b>	All	Major FW Rev	RO
<b>40 (Lower Page)</b>	All	Minor FW Rev	
<b>130 (Page 01)</b>	All	Major HW Rev	
<b>131 (Page 01)</b>	All	Minor HW Rev	

## 4 High Speed Signals

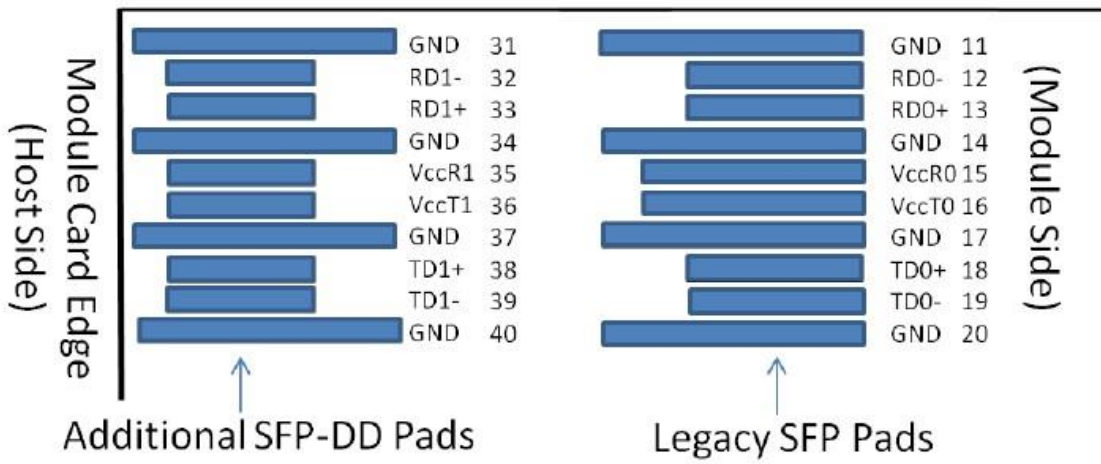
SFP-DD supports two lanes; TX0/RX0 and TX1/RX1. High speed signals are electrically looped back from TX side to RX side of the module, every differential TX pair is connected to its corresponding RX pair, and the signals are AC coupled as specified by SFP-DD MSA HW specs.

The Passive traces connecting TX to RX pairs are designed to support a data rate up to 28 Gbaud (56 Gbps).

## 5 ML4022-LB Pin Allocation



Bottom side as viewed from top thru board



Top side viewed from top of board

Figure 11: Module Pad Layout

## Revision History

Revision number	Date	Description
0.1	6/10/2019	▪ Preliminary
0.2	7/23/2019	▪ Correct description of low speed electrical hardware pins
0.3	8/13/2019	<ul style="list-style-type: none"> <li>▪ Section 3.6.5: Correct the values of power dissipation and the description in the table</li> <li>▪ Section 3.6.2: Update description of the three parameters</li> </ul>
0.4	1/29/2019	▪ Update cover page: specify version as V1
0.5	7/6/2020	<ul style="list-style-type: none"> <li>▪ Add ordering Part Number Paragraph</li> <li>▪ Add sections 3.6.5.1 and 3.6.5.2: power dissipation for different part numbers</li> </ul>
0.6	9/13/2021	▪ Format updates and proofreading

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